

## ABSTRACT OF THE INVENTION

5 A semiconductor memory of this invention is composed of  
an MFMS transistor including a first field effect transistor  
and a ferroelectric capacitor formed on or above the first  
10 field effect transistor with a gate electrode of the first  
field effect transistor working as or being electrically  
connected to a lower electrode of the ferroelectric capacitor,  
an upper electrode of the ferroelectric capacitor working as  
a control gate and the first field effect transistor having a  
15 first well region; and a second field effect transistor  
having a second well region that is isolated from the first  
well region of the first field effect transistor. The first  
well region of the first field effect transistor is  
electrically connected to the source region of the second  
field effect transistor, and the gate electrode of the first  
field effect transistor is electrically connected to the  
drain region of the second field effect transistor.

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